RECEIVED
CENTRAL FAX CENTER
SEP 14 2007

In the Claims:

Please amend claims 6, 8 and 18-19 as indicated below. This listing of claims replaces all prior versions.

1-5. (*Cancelled*)

6. (*Currently Amended*) An MIS type semiconductor device, comprising:

a semiconductor substrate,

a gate electrode formed on ~~the~~ a gate insulating film and formed of gate material, wherein the gate electrode comprises:

a first layer of activated crystalline gate material having a first side oriented towards [[a]] the substrate, ~~and~~ a second side oriented away from the substrate and a grain size, the first layer of activated crystalline gate material having a doping level of 10^{19} ions/cm^3 or higher, and

a second layer of gate material at the second side of the first layer of activated crystalline gate material, the second layer of gate material having a grain size,

wherein the grain size of the first layer of activated crystalline gate material is smaller than the grain size of the second layer of gate material.

7. (*Previously Presented*) A semiconductor device according to claim 6, wherein the first layer of activated crystalline gate material has a doping level of about 10^{20} ions/cm^3 or higher.

8. (*Currently Amended*) An MIS type semiconductor device according to claim 6, wherein ~~the~~ a doping implant in the activated gate material has an abruptness of a doping profile of about 2 nm or more.

9. (*Previously Presented*) A semiconductor device according to claim 6, wherein the second layer of gate material consists of amorphous gate material.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the Application:

Listing of Claims:

1. (currently amended) A thin film transistor array panel, comprising:

a substrate;

a gate line formed on the substrate and including a gate electrode;

a gate insulating layer formed on the gate line;

a semiconductor layer formed on the gate insulating layer;

a data line formed at least in part on the semiconductor layer;

a drain electrode formed on the semiconductor layer at least in part and separated from the data line;

a first passivation layer formed on the data line and the drain electrode;

a first protrusion formed directly on at least a portion of the first passivation layer and disposed on a portion corresponding to ~~opposite~~ the data line;

and,

a pixel electrode formed directly on the first passivation layer and connected to the drain electrode.

2. (original) The thin film transistor array panel of claim 1, wherein the pixel electrode has a cutout.

3. (original) The thin film transistor array panel of claim 2, further comprising a second protrusion disposed in the cutout.

4. (original) The thin film transistor array panel of claim 2, further comprising a storage electrode line overlapping the pixel electrode.

5. (original) The thin film transistor array panel of claim 4, wherein the storage electrode line comprises an expansion overlapping the drain electrode.

6. (original) The thin film transistor array panel of claim 4, wherein the storage elec-

trode line comprises a branch overlapping the cutout.

7. – 13. (cancelled)

14. (previously presented) A thin film transistor array panel, comprising:

a substrate;

a gate line formed on the substrate and including a gate electrode;

a gate insulating layer formed on the gate line;

a semiconductor layer formed on the gate insulating layer;

a data line formed at least in part on the semiconductor layer;

a drain electrode formed on the semiconductor layer at least in part and separated from the data line;

a first passivation layer formed on the data line and the drain electrode and having a contact hole exposing the drain electrode at least in part;

a pixel electrode formed directly on the first passivation layer and connected to the drain electrode through the contact hole, the pixel electrode having a cutout; and,

a protrusion formed directly on at least a portion of the first passivation layer and disposed in the cutout at least in part.

15. (original) The thin film transistor array panel of claim 14, further comprising a storage electrode line overlapping the pixel electrode.

16. (original) The thin film transistor array panel of claim 15, wherein the storage electrode line comprises an expansion overlapping the drain electrode.

17. (original) The thin film transistor array panel of claim 15, wherein the storage electrode line comprises a branch overlapping the cutout.

18. (cancelled)

19. (original) The thin film transistor array panel of claim 14, further comprising a spacer having a height larger than the protrusion and disposed on the same layer as the protrusion.

20. (original) The thin film transistor array panel of claim 19, wherein the protrusion and the spacer comprise organic material.

21. (previously presented) The thin film transistor array panel of claim 14, comprising a color filter disposed between the first passivation layer, and the protrusion and the pixel electrode.

22. (previously presented) The thin film transistor array panel of claim 21, further comprising a second passivation layer formed on the color filter and intermediate to the protrusion and the pixel electrode.

23. (previously presented) The thin film transistor array panel of claim 14, wherein the semiconductor layer has substantially the same planar shape as the data line and the drain electrode.

24. – 27. (cancelled)